09/899,413

1. (Amended) A method for evaluating gate timing in an integrated circuit (IC) design, said method comprising:

determining when a first-type of signal is present on an input to a logical gating device, wherein said first-type of input signal allows transitions on an output of said gating device;

determining when a second-type of signal is present on said input, wherein said second-type of input signal inhibits transitions on said output of said gating device; and

modifying a timing of a sensing of said first-type of signal to sense said first-type of signal at an earlier point in time than said second-type of signal is sensed.

3. (Amended) The method of claim 1, wherein:

said input comprises a clock input;

said first-type of signal and said second-type of signal comprise clock trailing edge signals;

said first-type of signal causes a transition at said output of said gate device due to a transition on a gate input of said gate device; and

said second-type of signal prevents a transition at said output of said gate device.

4. (Amended) The method of claim 2, wherein said first-type of signal [prevents] allows said clock pulses to be propagated on said output of said gating device and said second-type of signal prevents said clock pulses from being propagated on said output of said gating device.

11. (Amended) A method for evaluating gate timing in an integrated circuit (IC) design, said method comprising:

determining when a first-type of signal is present on an input to a logical gating device, wherein said first-type of input signal allows a clock pulse to be output from said gating device;

determining when a second-type of signal is present on said input, wherein said second-type of input signal inhibits said clock pulse from being output from said gating device; and

modifying a timing of a sensing of said first-type of signal to sense said first-type of signal at an earlier point in time than said second-type of signal is sensed.

17. (Amended) A program storage device readable by machine, tangibly embodying a program of instructions executable by said machine for performing a method of evaluating gate timing in an integrated circuit (IC) design, said method comprising:

determining when a first-type of signal is present on an input to a logical gating device, wherein said first-type of input signal allows transitions on an output of said gating device;

determining when a second-type of signal is present on said input, wherein said second-type of input signal inhibits transitions on said output of said gating device; and

modifying a timing of a sensing of said first-type of signal to sense said first-type of signal at an earlier point in time than said second-type of signal is sensed.

19. (Amended) The program storage device of claim 18, wherein said first-type of signal allows said clock pulses to be propagated on said output of said gating device and said second-type of signal prevents said clock pulses from being propagated on said output of said gating device.